Digital Array Radar: MPAR Applications

Dr. William Chappell, Caleb Fulton

Purdue University

Sponsored by:

CERDEC US ARMY – RDECOM

Collaboration with CREE Semiconductor, Lockheed Martin, and Sierra Monolithics

Overview of Presentation

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Cost is a risk for the MPAR program

- Introduction
  - Trends in Electrical Engineering
  - What is a Digital Array Radar
- Current DAR Effort
  - Approach
    - GaN/ SiGE two chip channels
  - Results
- Weather-Specific Related Issues
  - Dual Polarization
- Low Cost Perspectives

Trends in Electrical Engineering

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To create a low cost radar it seems imperative to leverage the trends occurring at the component level.

A.) Massively Integrated RF Components, System on Chip.
-SiGe and CMOS RFIC's

B.) Widebandgap Semiconductors
-GaN and SiC – III-V semiconductors

C.) Severe Impact from Digital Portion of Systems
-Calibration, adaptability, and correction by feedback from the digital domain

What is a Digital Array Radar?

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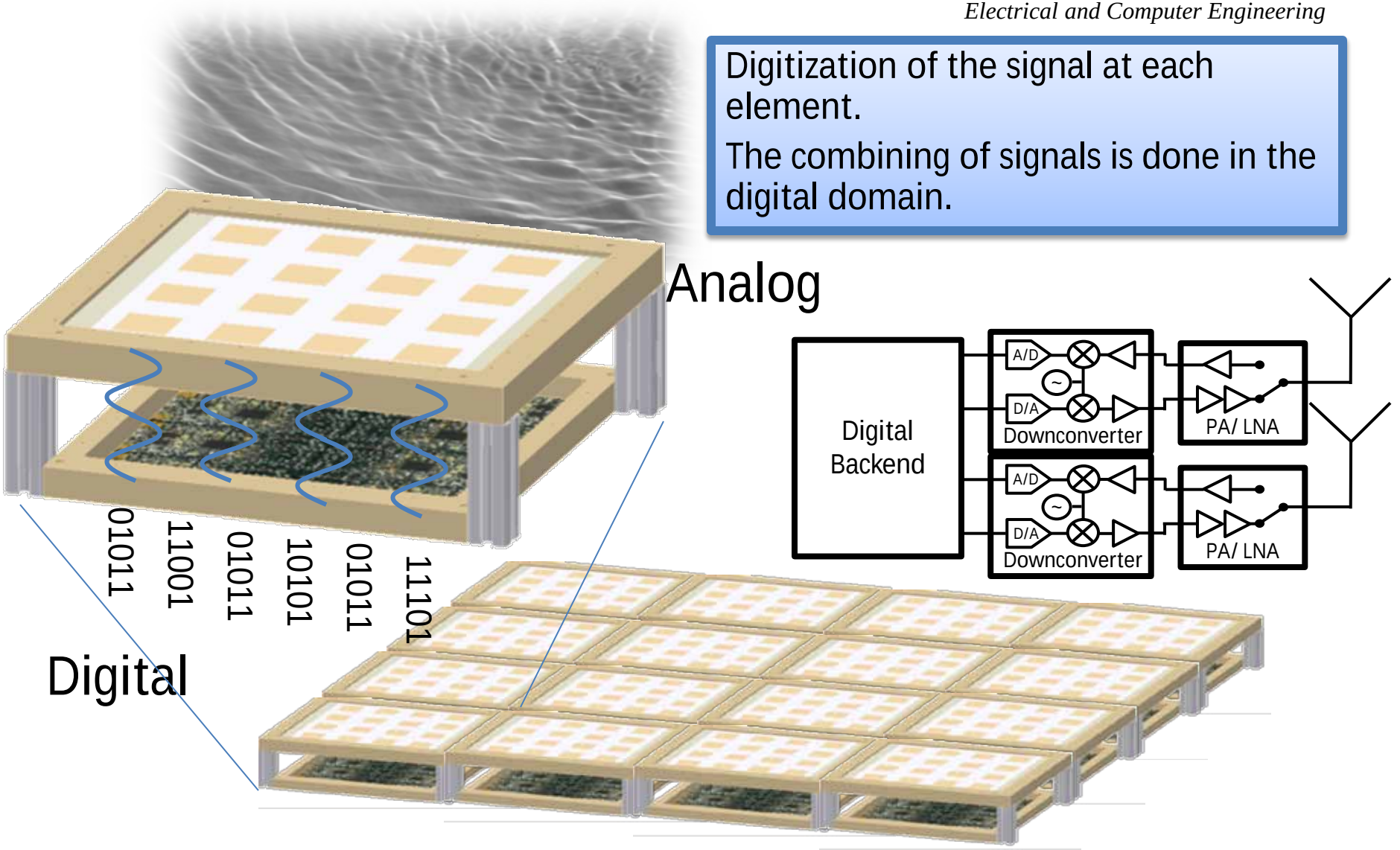
Digitization of the signal at each element.

The combining of signals is done in the digital domain.



DAR Program Concept V0

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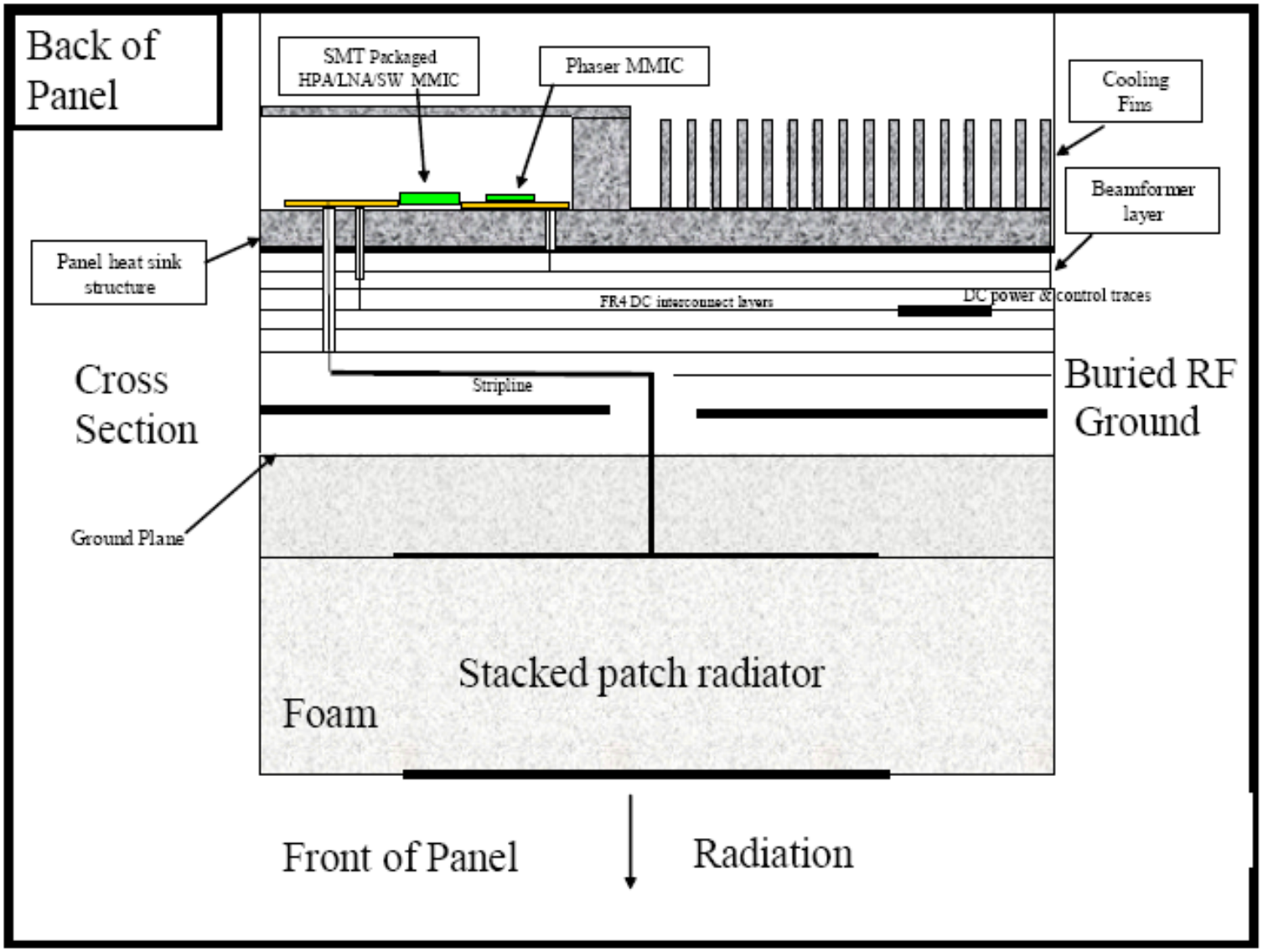
GaN and SiGe

Traditional Multilayer Board

Antenna



Initial Concept

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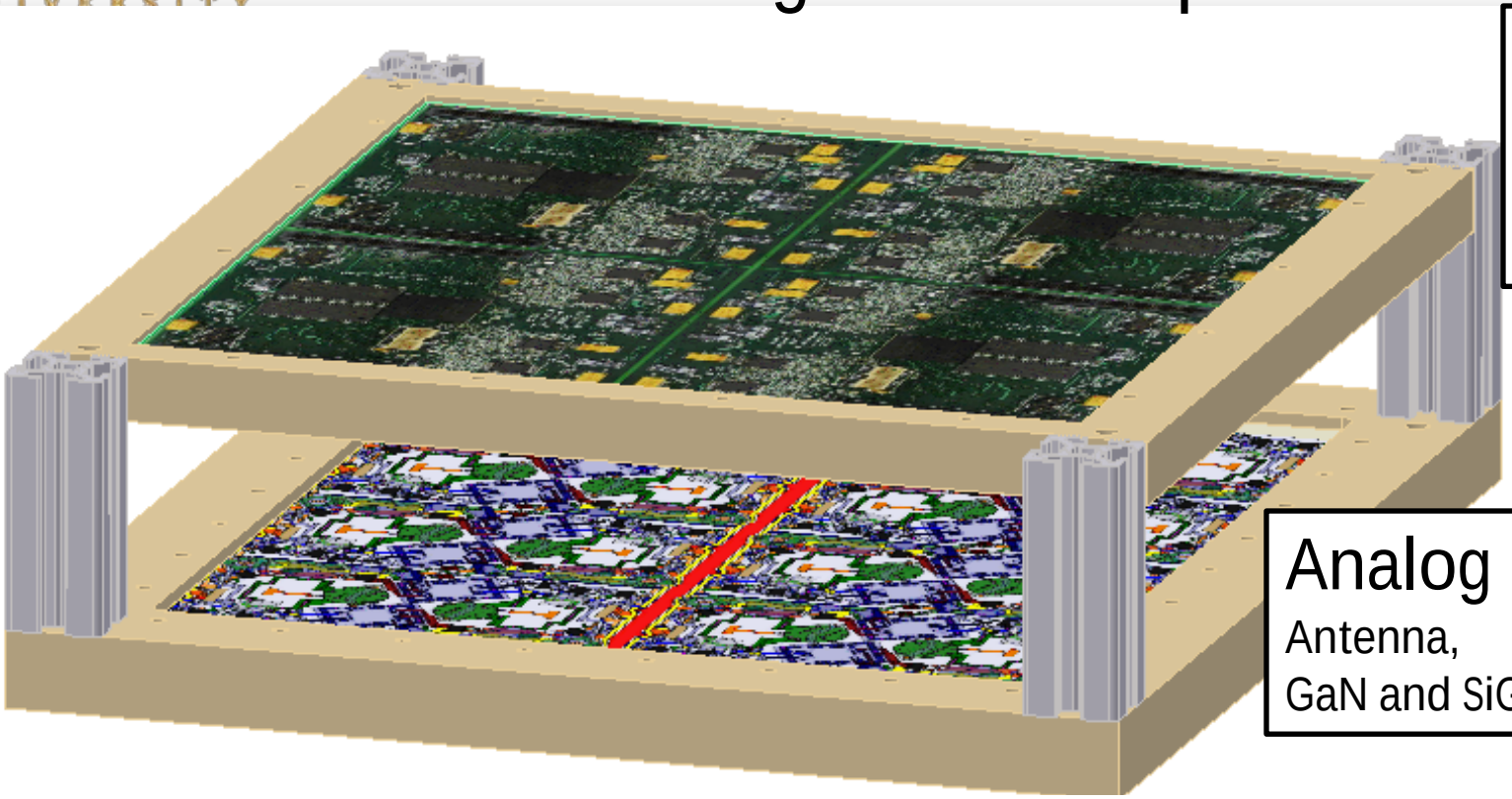
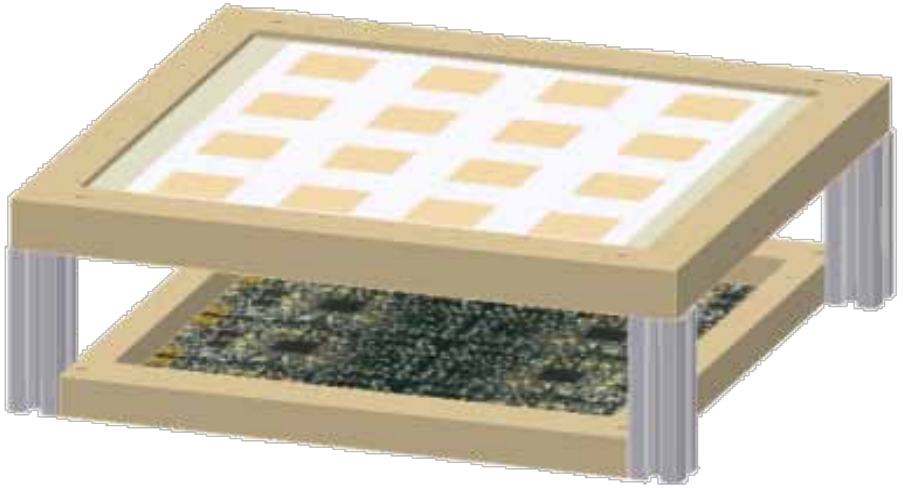
DAR Program Concept V1



Digital
ADC/DAC's,
FPGA's,
Memory

Analog
Antenna,
GaN and SiGe

CAD Representations of
Final Prototype Subarray



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DAR Program Demonstrator

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Measured DAR Version I Prototype Subarray

On display outside for dual polarization.
A thorough overview and demo is planned at 1 PM in 1350 NWC (Next door)

Low-Cost DAR Radar

"2 Chip Radar" Solution

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Traditional Hybrid Radar Module

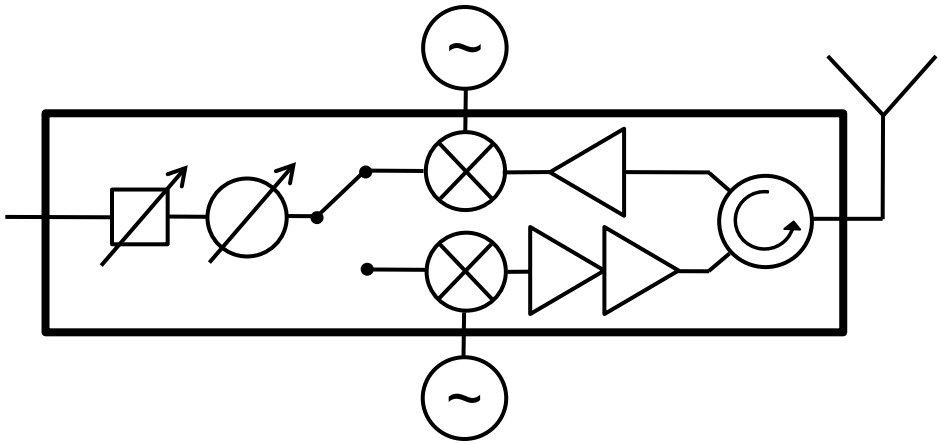
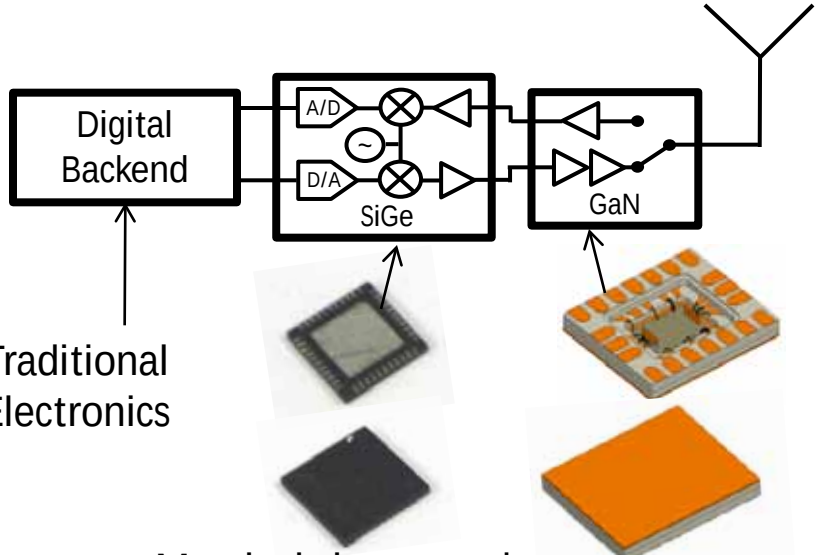


Image from Eurofighter's radar
http://www.airpower.at/news06/0922_captor-e/index.html

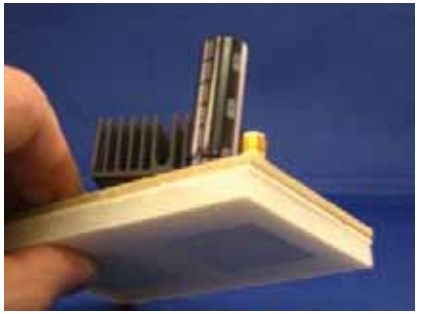
Advanced Integration



Traditional Electronics

Massively integrated SiGe chip transceivers

High Power GaN MMIC



Planar "laptop-like" Integration – Simple 4 Layer Board for Analog Components

Remove Component Cost By Leveraging Commercial Integration Practices, remove T/R module

The 400 Watt Radiating "Laptop" Panel

Digital Beamforming Architectures

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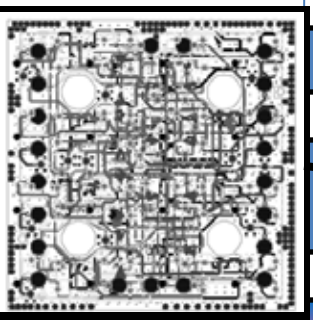
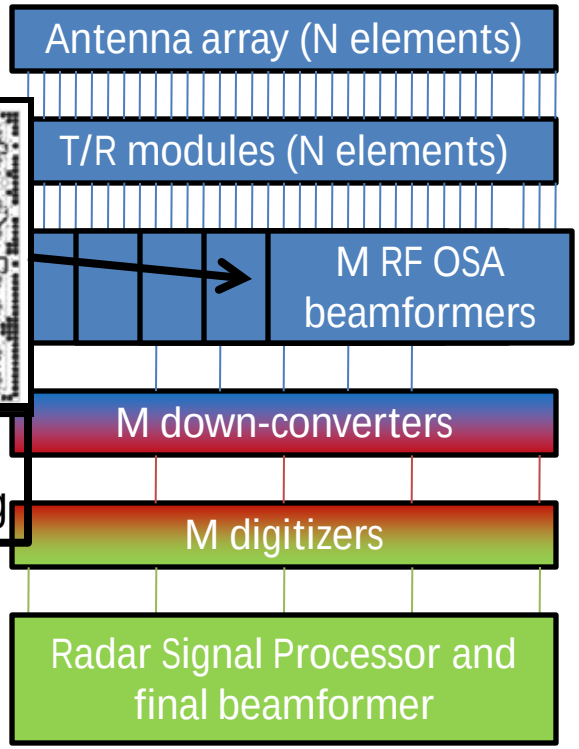
Overlapped Subarray (OSA) Digitization

Can form on the order of M simultaneous beams with purely analog beamformers



Analog Beamforming



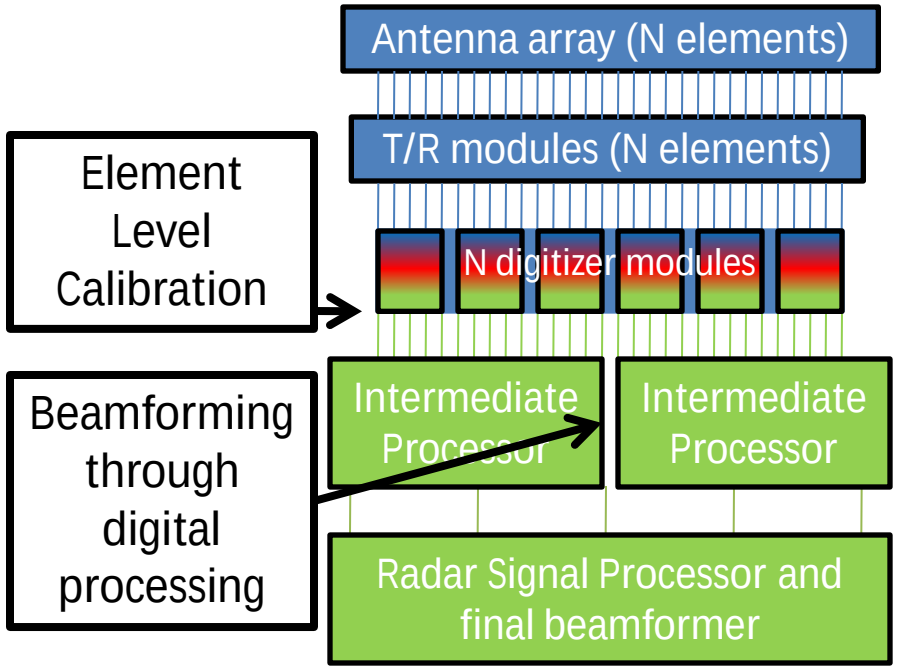
RF

Baseband

Digital

Digital at Every Element with Hierarchical Digital Backend

Digitizer modules, intermediate processors, and final signal processor work together intelligently and flexibly



High Power Plastic Antenna Array

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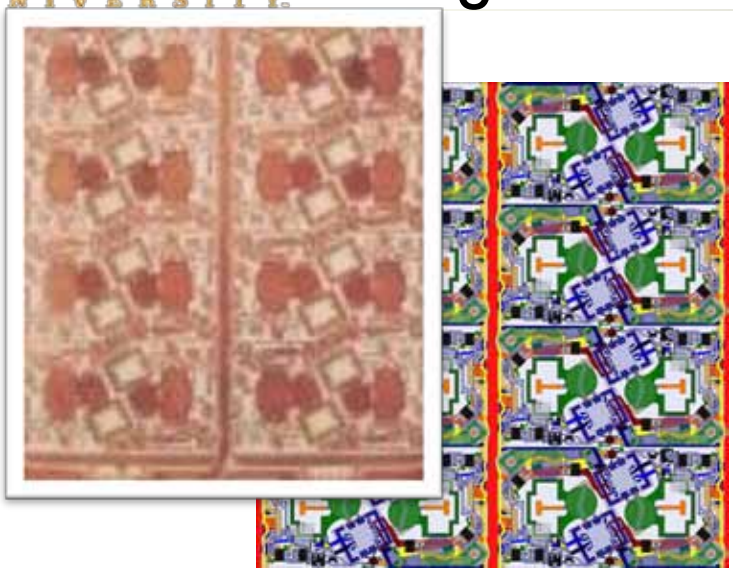

16 element panel

Composite multilayer polymer antenna

Large Area Integration
8x8 antenna only array constructed

- ***>35 Watts per element has been demonstrated with limited cooling on RF GaN antenna panel***
- **Air cooling upto 50 % duty cycle with 25 watts radiated**
- **Simulations show 80% efficiency at 7 Watts for GaN Amplifiers for 2.7 to 2.9 GHz**
- **Plastic QFN packages are therefore possible**

GaN Results

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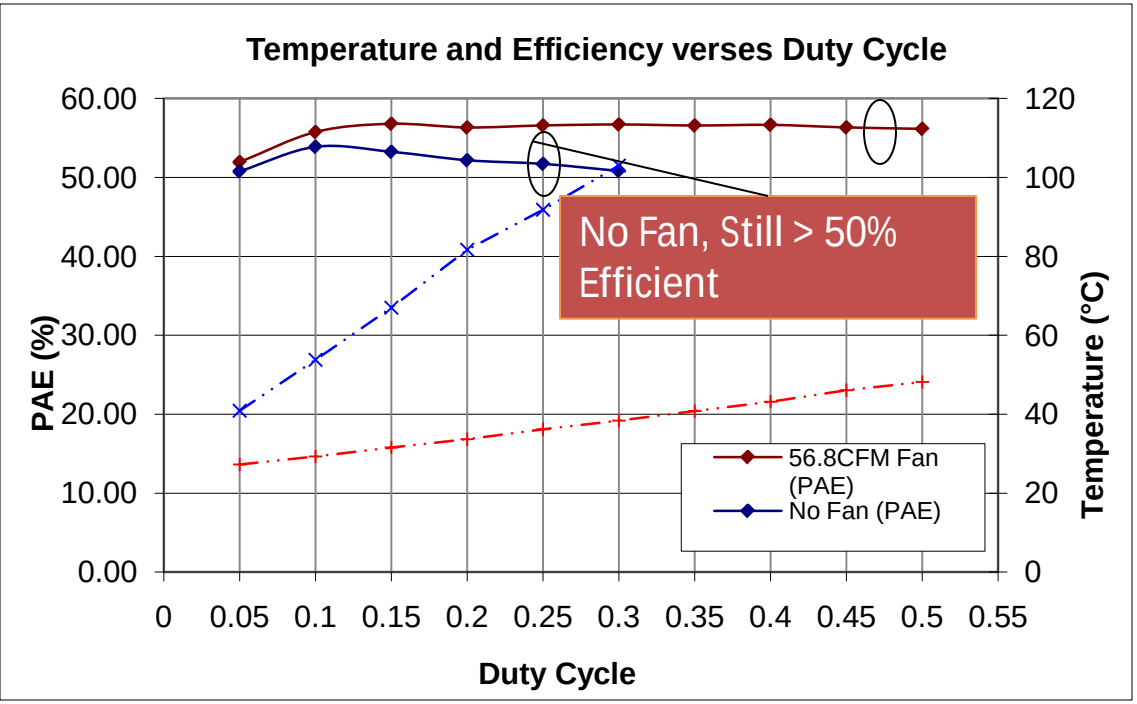
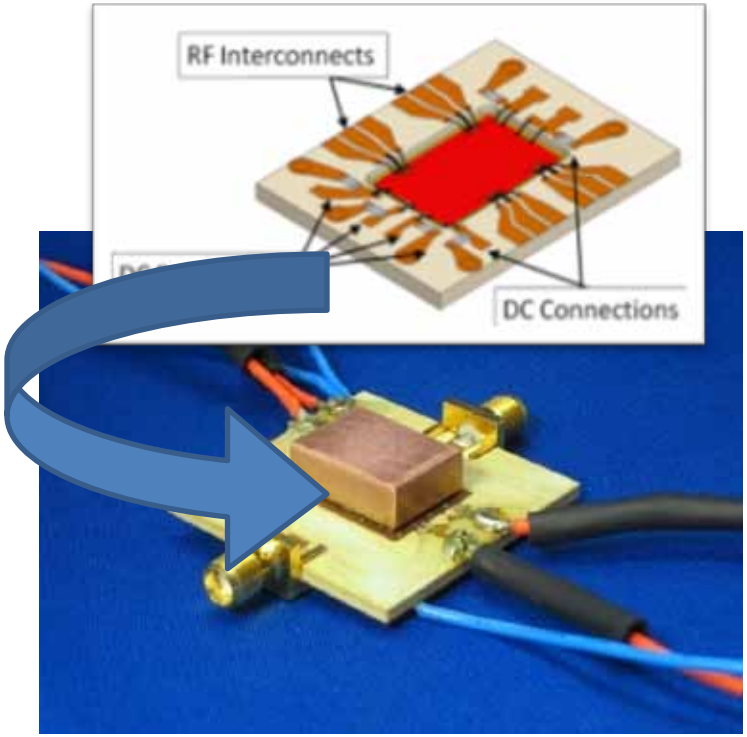
Cost is Reduced Through Simplified Packaging

- Comparison of Air Cooling Techniques
- At least 10°C cooler than without a fan
- All tested points above 22dB of Gain
- Base Plate (Solid), Input Stage (Dash) and Output Stage (Dash-Dot)

Plastic Packaging and Simple Cooling Enabled through the Efficient Modes of Operation





Up to 50 Watts Demonstrated in a Plastic Package

10W Ultra-High Efficiency MMIC PA

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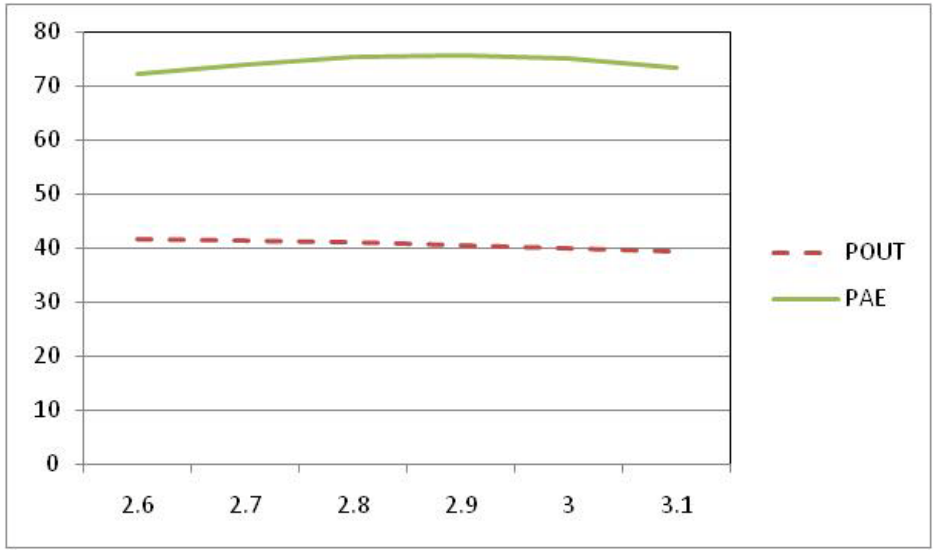
Simulated MPAR MMIC Performance



- 2-Stage GaN MMIC
- 2 mm output stage
- 2.7-3.1GHz operation
- 50 Ohm In/Out
- Est. Chip Size = <4 mm^2
- RF P_{OUT} = 10 Watts
- PAE = 75%
- Large Signal Gain = 28dB
- Drain voltage = 28 volts
- Est. Production Cost: ~$12/chip

Cree GaN Process capable of supporting ultra-high efficiency MPAR power amps

Solid State Trends

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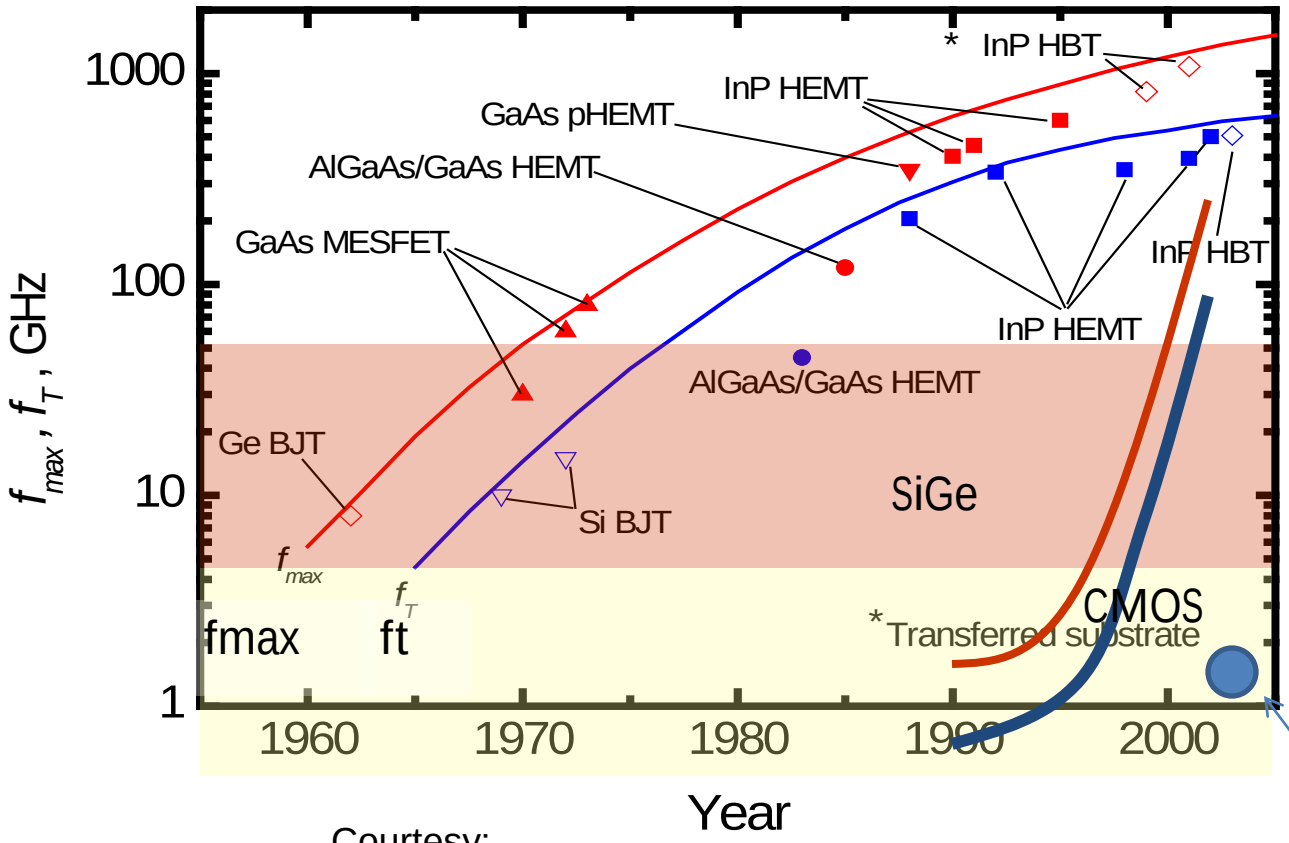

Courtesy:
www.eas.asu.edu/~vasilesk/EEE532/Talk_ASU_short.ppt

MPAR is easily within the range of silicon IC's

Important Solid State Trends:

- Continuous increase of the frequency limits, i.e. f_T and f_{max} (III-V's)
- Increase of output power (wide bandgap transistors)
- Low-cost RF transistors for consumer mass markets (Si-based)

mm-wave Silicon

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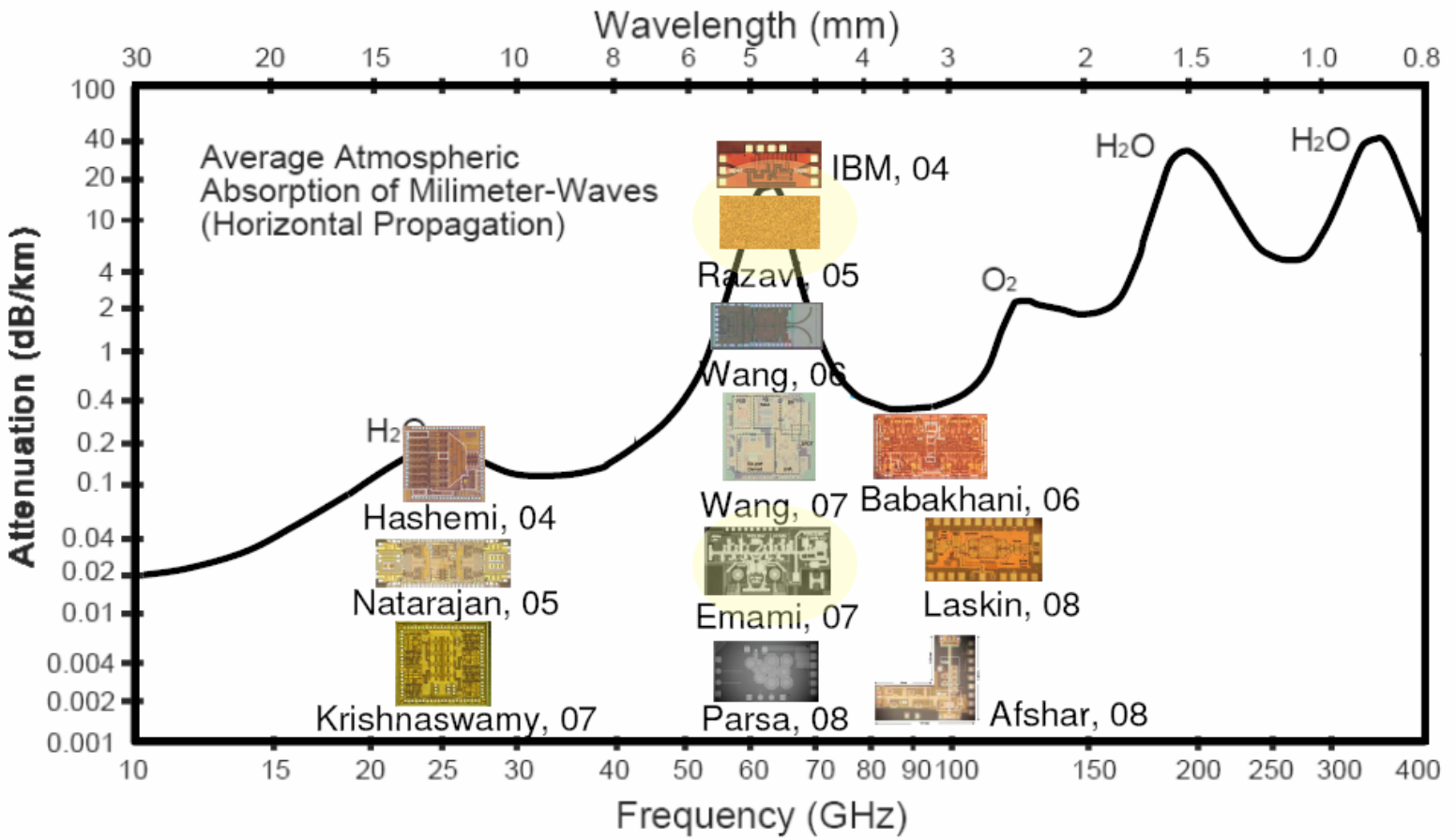
The mm-"Wave" in Industry and Academia



Fully-integrated mm-wave transceivers reported at ISSCC.

Courtesy of Harish Krishnaswamy at USC

Promise of the Technology

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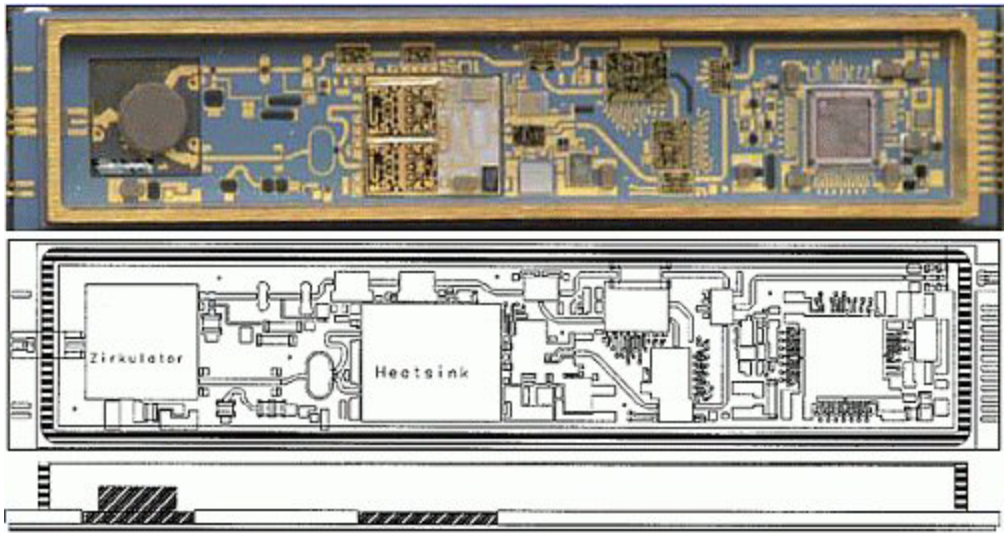
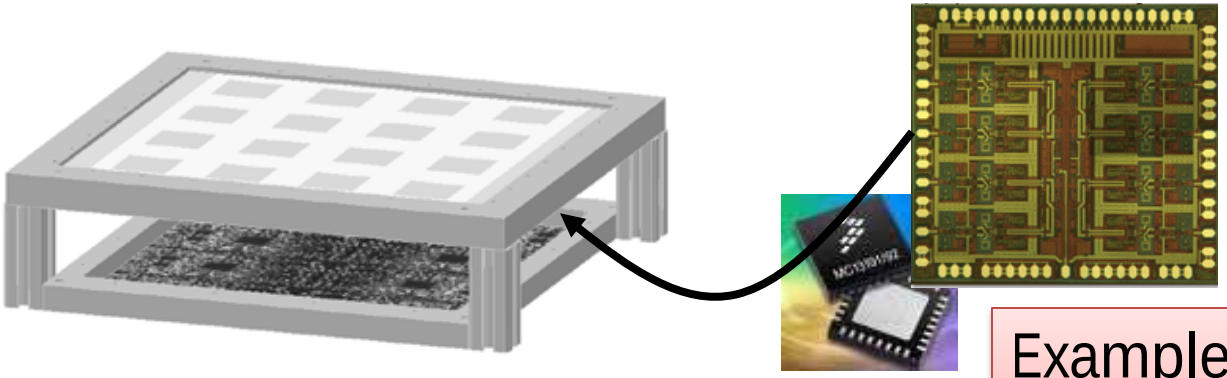
- Recent Demonstrations – 8 element receive only array that is 2 by 3 mm in Jazz .18 micron SiGe – Works from 6 to 18 GHz (UCSD)



Multichip Module
Replaced by
Multireceiver Silicon IC



Example of 16 elements on a chip

"motherboard-like RF array integration"

Two-Channel SiGe Transceiver

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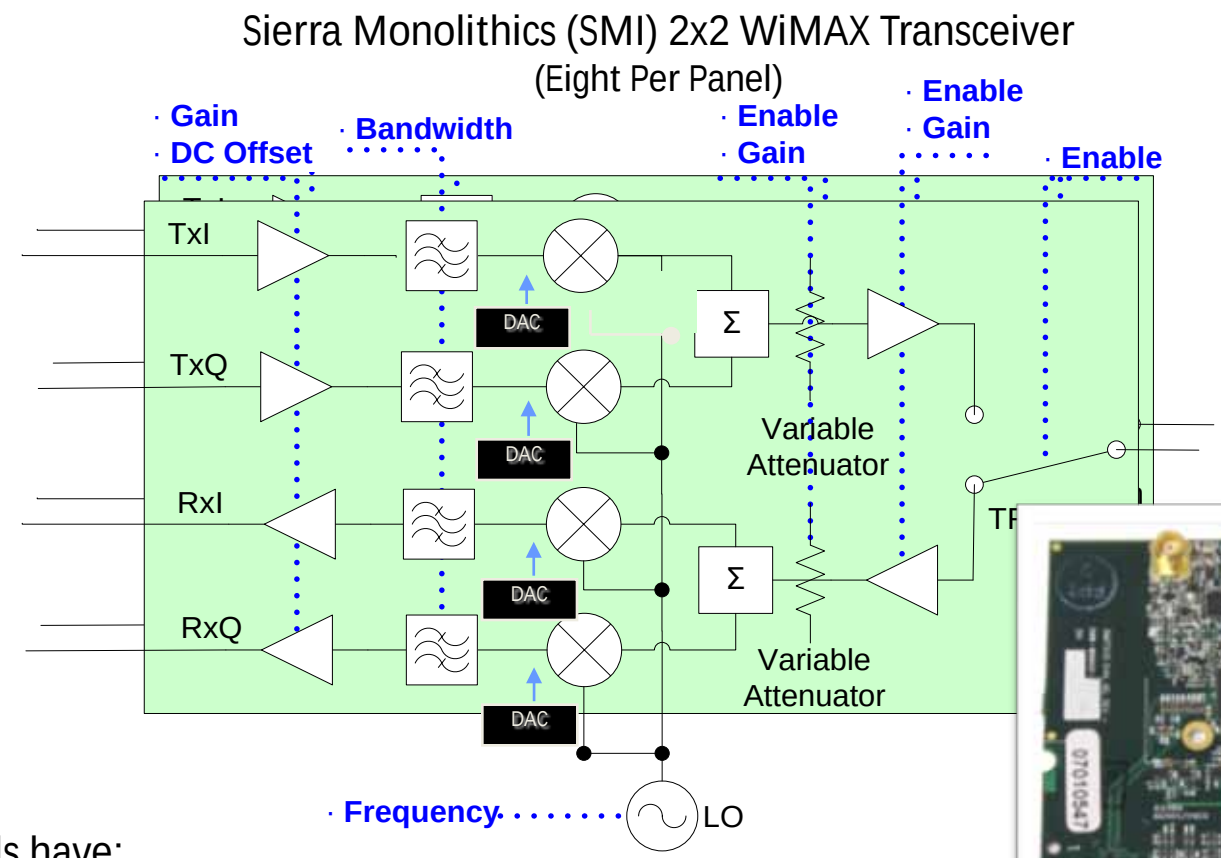
SiGe integration allows for more than 1 radar channel per chip. Beyond (SOC) System on Chip



- SMI boards have:
  - Two independent direct-conversion I/Q Tx/Rx channels per board
  - 54 programmable registers
  - Flexibility in gain, filtering, DC offset compensation, etc.
  - Programmable RF LOs on each board

Tracking Demonstration

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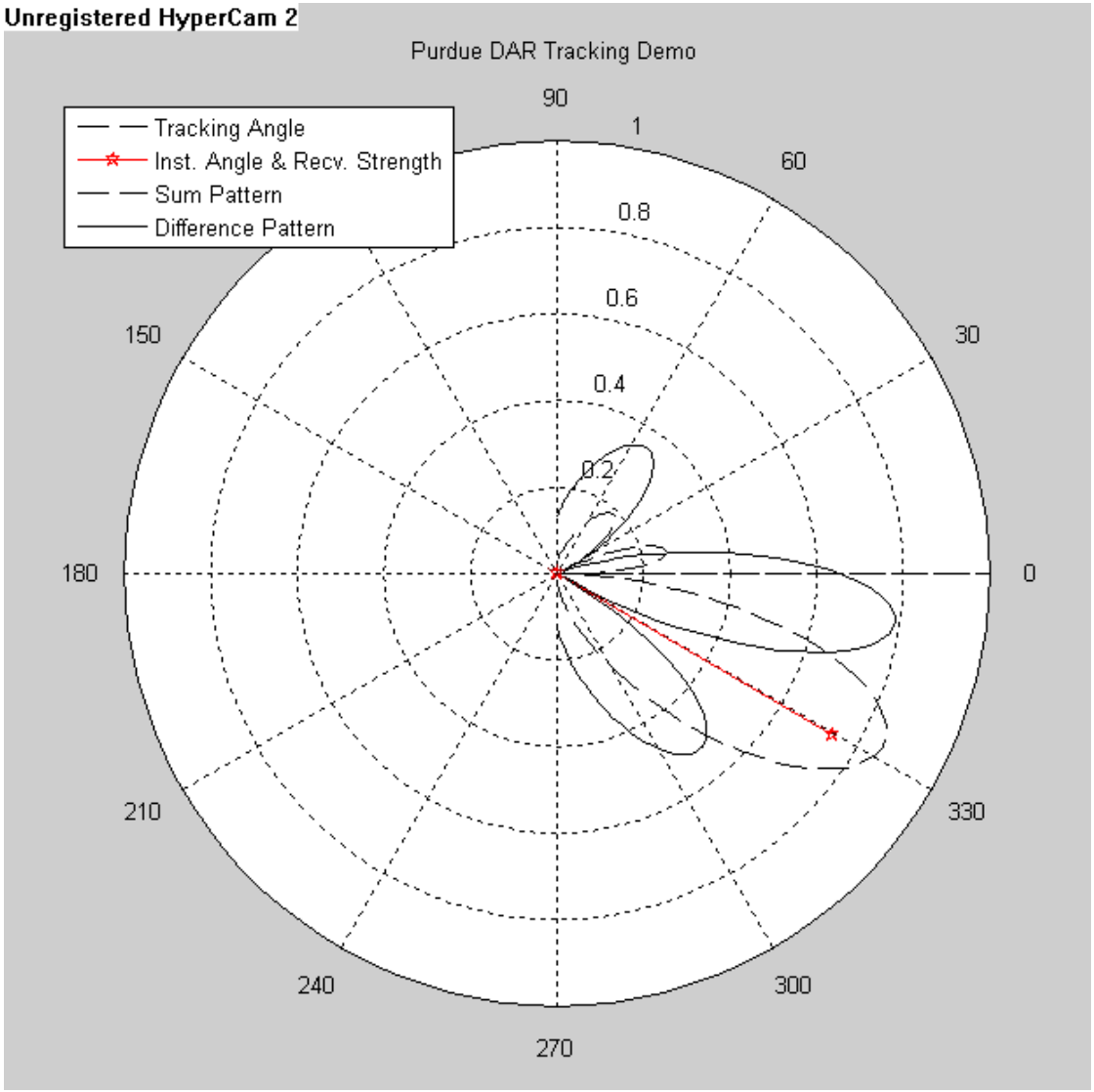

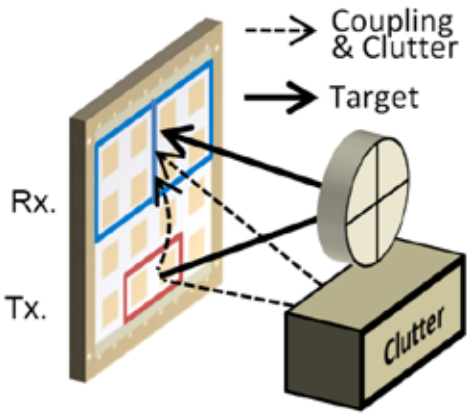

Tracking demonstrated using digital beamformer

Dual Polarization Variation of DAR

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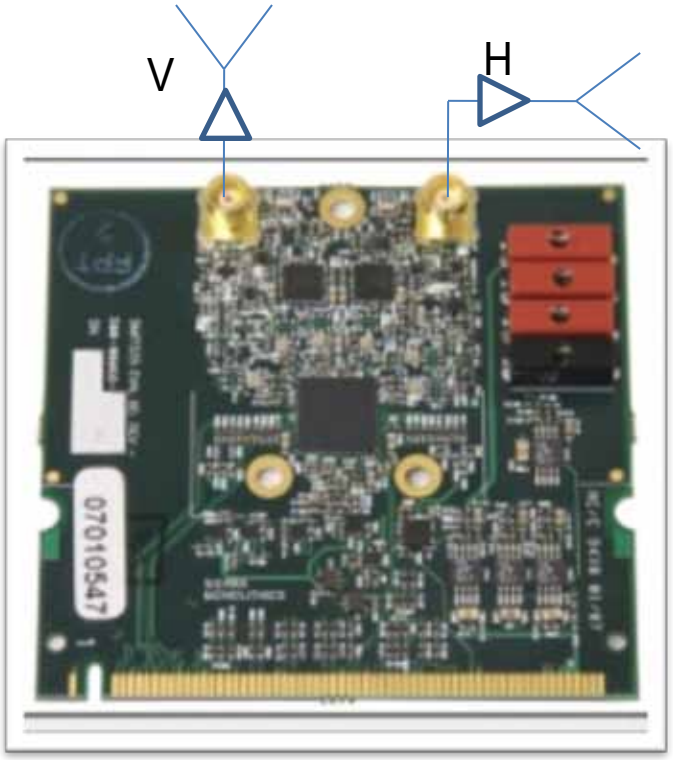
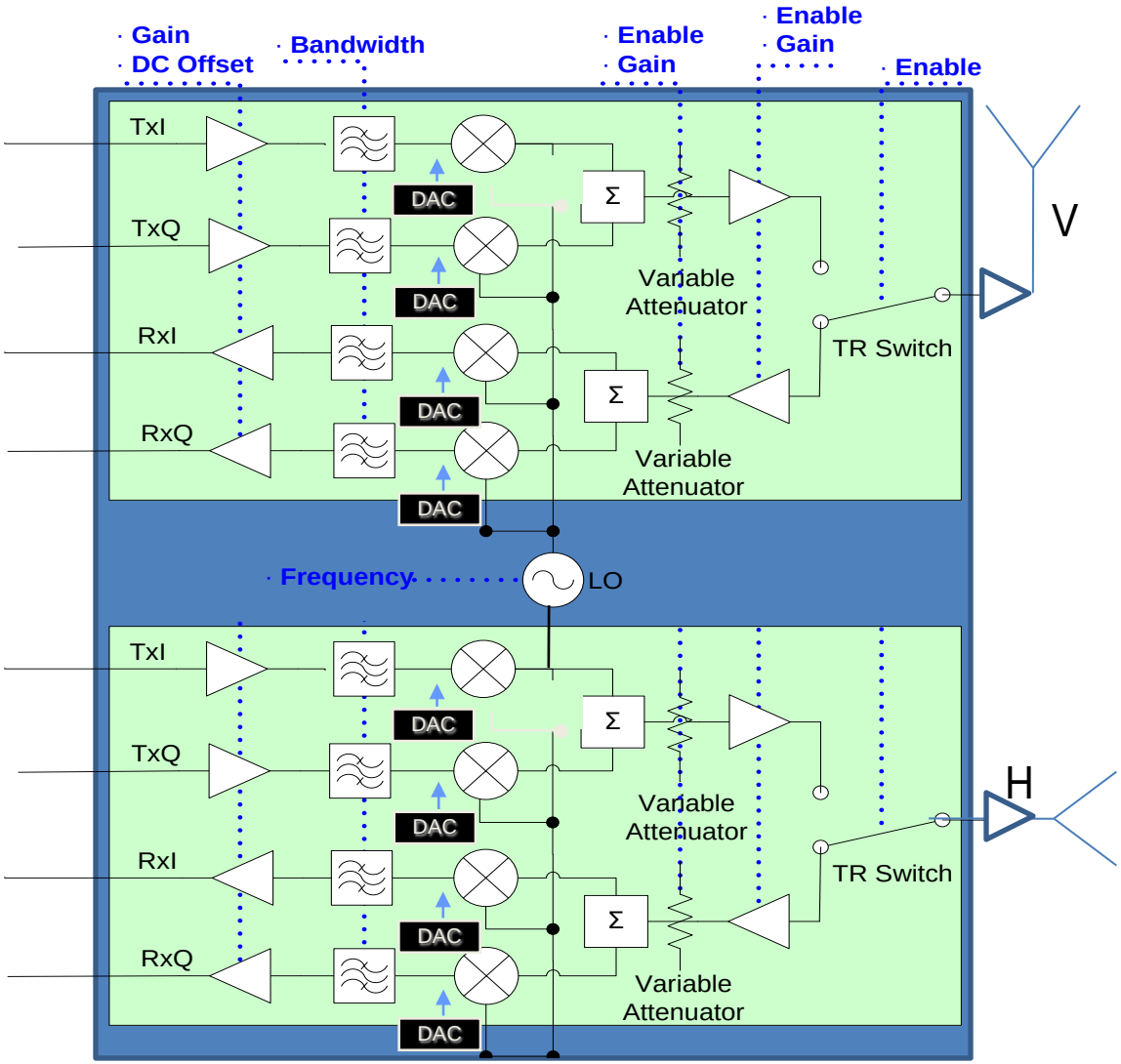
The integrated SiGe transceiver is very useful for dual polarization

There are two channels on one integrated circuit, so one IC handles both inputs from the antennas.



Direct Data Output



DAR Dual Polarization Work

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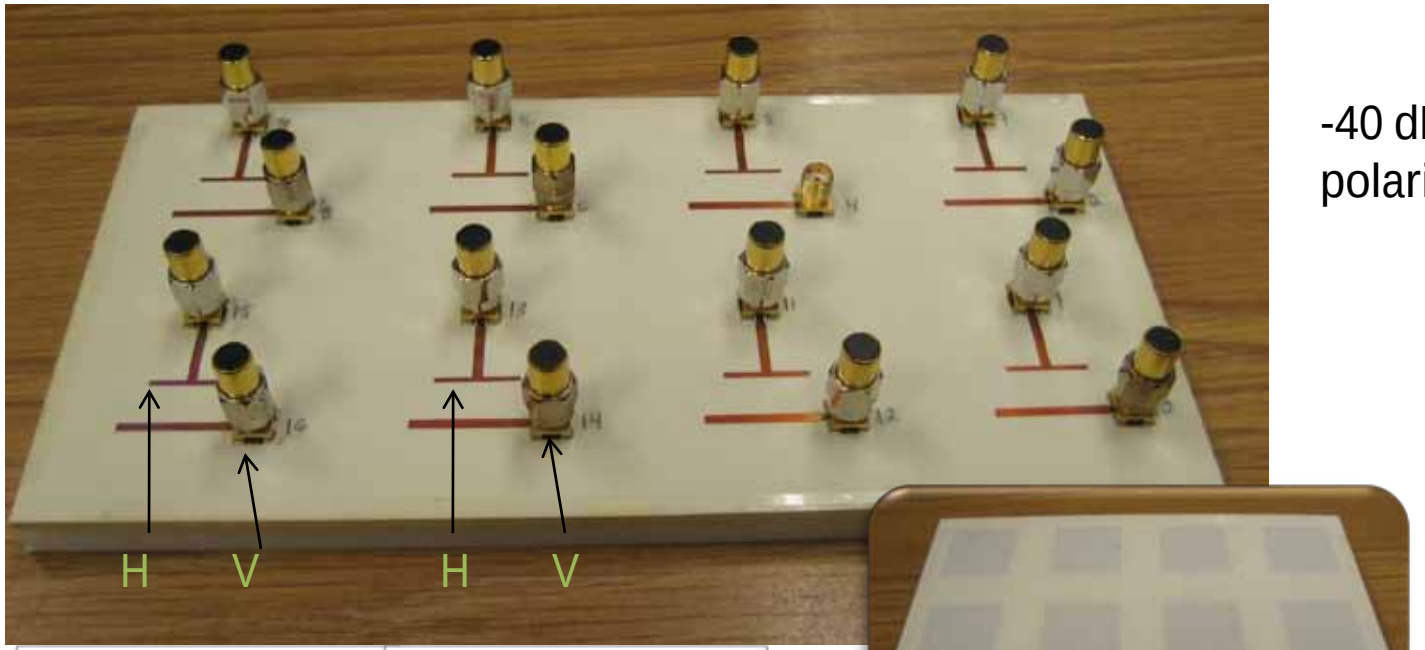
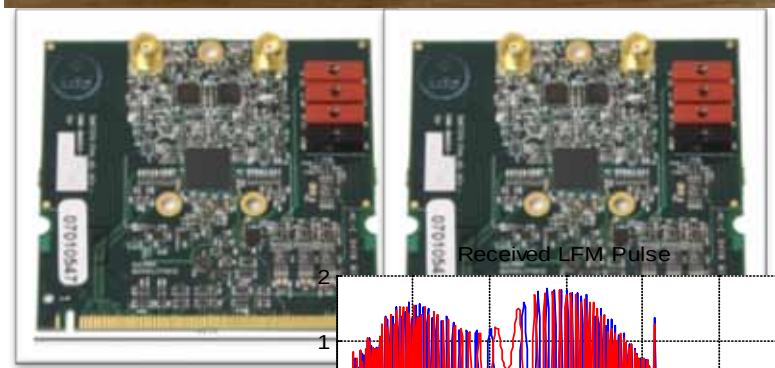
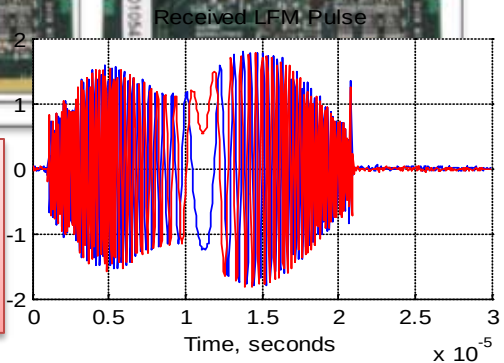


-40 dB isolation between polarizations





Measured V and H data of LFM pulse

Measured simultaneous transmit on each polarization

Independent waveform synthesis at each antenna will allow for compensation of polarization mismatches to improve polarization metrics

Conclusion

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- Cost is a risk for the MPAR program

- Leveraging the advances at the component level will be useful for pushing the cost curve down

  - Massive Integration - SiGe
  - High Power Plastic Operation – GaN
  - Digital Utilization – Digital at Every Element
    - -Let the broader electronics world do the heavy lifting

Digital at every element has been demonstrated for a 16 element panel.

A low cost phased array can be built if commercial trends and practices are leveraged.

A detailed overview of the array and a demonstration of the performance will be shown at 1 PM in room

Next door, 1 PM

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DAR Version I Subarray Architecture

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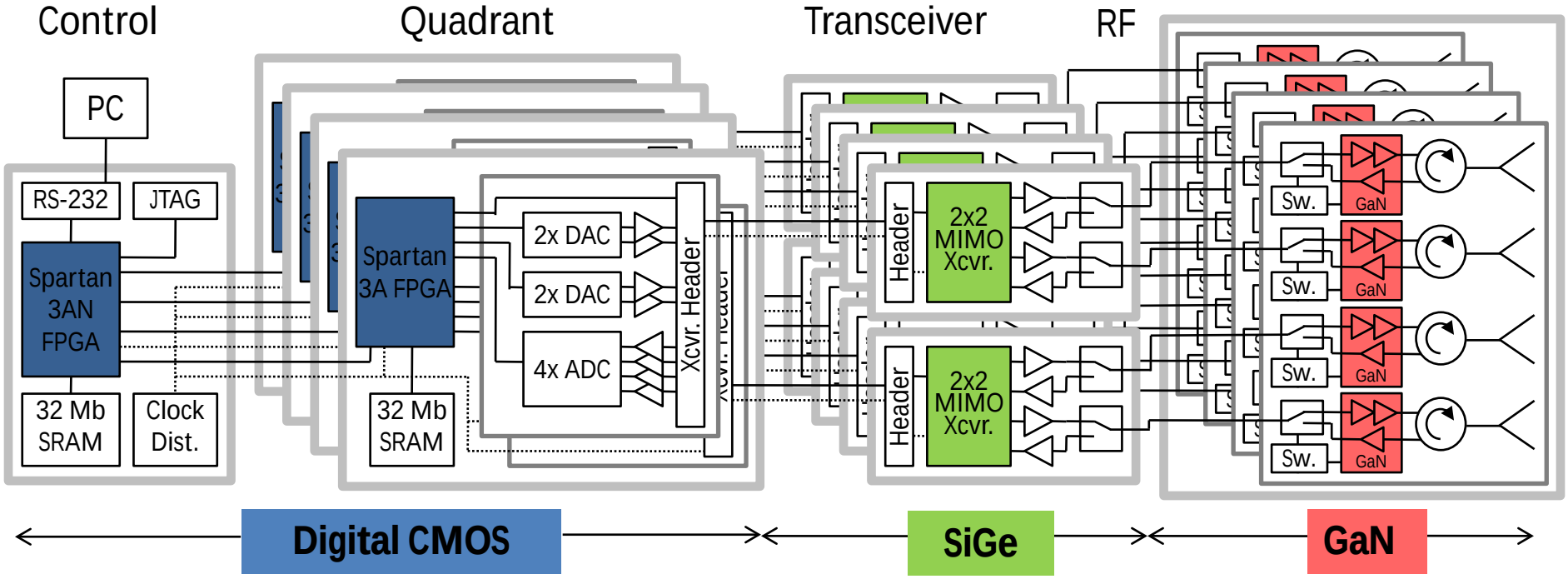

5) *Synchronization*
Digital backend Control board designed, laid out, and populated in-house

Wrote firmware for FPGAs and software for host PC interface

3) *Silicon Integration* Utilized integrated Sierra Monolithics 2x2 WiMAX SiGe transceiver

4) *Digital Processing* Quadrant boards perform data conversion and element-level processing

1) *Antenna Panelization* Antenna was designed, analyzed for mutual coupling, fabricated, and tested

2) *Plastic High Power Packaging* Multi-layer panel and plastic packaging designed to house efficient GaN T/R modules